Amendments to the Claims

1 - 10 (canceled)

11. (currently amended) A digital filter ~~that filters an input data stream which provides data elements at a system rate F_S, the filter~~ comprising[[;]] :

a divider that responds to an input clock signal that has an input rate and provides a reduced clock signal that has a reduced rate;

at least one buffer register that receives an input data stream of data elements and provides a delayed data stream;

at least two latches arranged to receive respective ones of said input and delayed data streams and provide latched data substreams in response to said reduced clock signal; and

at least two convolvers that each receive said data substreams wherein each convolver includes:

a) buffer registers that receive and successively delay data elements of said data substreams;

b) digital multipliers arranged to multiply received data elements and data elements from said buffer registers with stored filter coefficients to thereby provide products; and

c) digital summers that sum said products to generate an output data signal

~~a converter that converts successive strings of M successive data elements in said input data stream to M parallel data elements that occur at a substream rate F_S/M in M data substreams; and~~

~~a data processor programmed to generate, at said substream rate F_S/M, M convolutions of a quantized impulse response with said M data substreams~~.

12 - 15 (canceled)

16. (currently amended) The filter of claim 11, further including a multiplexer that receives output data signals from respective convolvers and, in response to said input clock signal, combines them into an output data stream ~~multiplexes said convolutions at said system rate F_S~~.

17 - 20 (canceled)

21. (currently amended) A digital filter ~~that filters an input data stream which provides data samples at a system rate F_S, the filter~~ comprising[[;]] :

a divider that responds to an input clock signal that has an input rate and provides a reduced clock signal that has a reduced rate;

at least one buffer register that receives an input data stream of data elements and provides a delayed data stream;

at least two latches arranged to receive respective ones of said input and delayed data streams and provide data substreams in response to said reduced clock signal;

for each respective one of said data substreams, a set of buffer registers that receive and successively delay data elements of said respective data substream;

multipliers arranged to multiply received data elements and data elements from said buffer registers with stored filter coefficients to thereby provide products; and

for each respective one of said data substreams, a set of summers arranged to sum said products and thereby generate an output data signal

~~a converter that converts successive strings of M successive data elements in said input data stream to M parallel data elements that occur at a substream rate F_S/M in M data substreams; and~~

~~M convolvers which generate, at said substream rate F_S/M, M convolutions of a quantized impulse response with said M data substreams.~~

22 - 23 (canceled)

24. (currently amended) The filter of claim 21, further including a multiplexer that receives each output data signal and, in response to said input clock signal, multiplexes all output data signals into an output data stream ~~multiplexes said convolutions at said system rate F_S~~.

25 - 26 (canceled)

27. (new) A digital filter, comprising:

a divider that responds to an input clock signal that has an input rate and provides a reduced clock signal that has a reduced rate;

a buffer store that receives an input data stream of data elements and provides at least one delayed data stream;

at least two latches arranged to receive respective ones of said input and delayed data streams and provide latched data substreams in response to said reduced clock signal; and

at least one data processor programmed to convolve each of said data substreams with stored filter coefficients to thereby generate a respective one of output data signals.

28. (new) The digital filter of claim 27, further including a multiplexer that receives said output data signals and, in response to said input clock signal, multiplexes them into an output data stream.

29. (new) The digital filter of claim 27, wherein said processor is further programmed to receive and successively delay data elements of each of said data substreams, multiply received and delayed data elements with stored filter coefficients to provide products, and, for each of said data substreams, sum respective products to generate a respective one of said output data signals.